NEC

MOS FIELD EFFECT TRANSISTOR
μPA1840

N-CHANNEL MOS FIELD EFFECT TRANSISTOR FOR SWITCHING

DESCRIPTION

The μPA1840 is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for high voltage applications such as DC/DC converter.

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1840GR-9JG	Power TSSOP8

FEATURES

- High voltage rating V_{DSS} = 200 V
- Power TSSOP8 package (Single circuit)
- Gate voltage rating ±30 V
- Low on-state resistance
  $R_{DS(on)}$ = 0.53 Ω MAX. (V_{GS} = 10 V, I_D = 1.5 A)
- Low input capacitance
  C_{iss} = 320 pF TYP. (V_{DS} = 10 V, V_{GS} = 0 V)
- Built-in gate protection diode

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	200	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±30	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±3.0	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±9.0	A
Total Power Dissipation Note2	P_T	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1 %

2. Mounted on ceramic substrate of 5000 mm^2 x 1.1 mm

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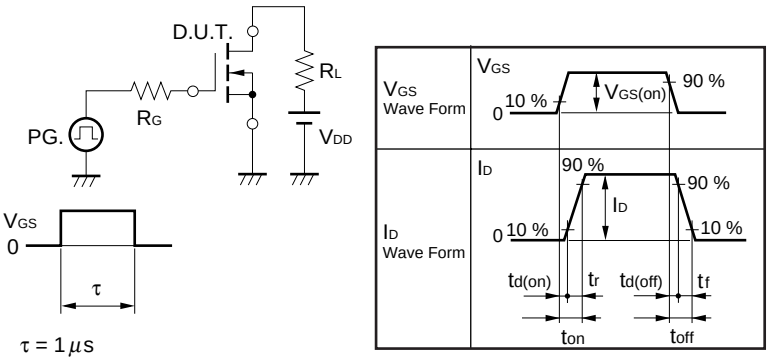
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

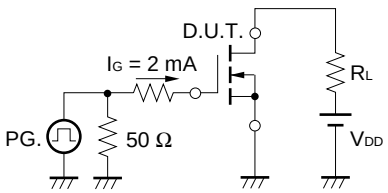
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Leakage Current	I_{DSS}	V_{DS} = 200 V, V_{GS} = 0 V			100	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	2.5		4.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 1.5 A	1.2			S
Drain to Source On-state Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 1.5 A		0.4	0.53	Ω
Input Capacitance	C_{iss}	V_{DS} = 10 V		320		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		88		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		44		pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 1.5 A		9.6		ns
Rise Time	t_r	$V_{GS(on)}$ = 10 V		20		ns
Turn-off Delay Time	$t_{d(off)}$	V_{DD} = 100 V		36		ns
Fall Time	t_f	R_G = 10 Ω		16		ns
Total Gate Charge	Q_G	I_D = 3.0 A		12		nC
Gate to Source Charge	Q_{GS}	V_{DD} = 160 V		2.8		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = 10 V		8.0		nC
Diode Forward Voltage	$V_{F(S-D)}$	I_F = 3.0 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 3.0 A, V_{GS} = 0 V		200		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 50 A/μs		0.8		μC

TEST CIRCUIT 1 SWITCHING TIME



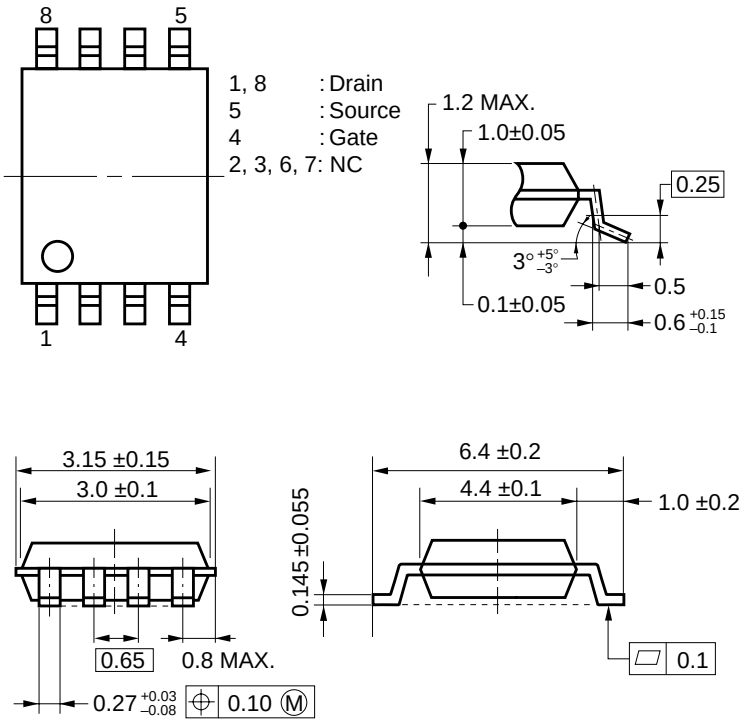
τ = 1 μs
Duty Cycle ≤ 1 %

TEST CIRCUIT 2 GATE CHARGE



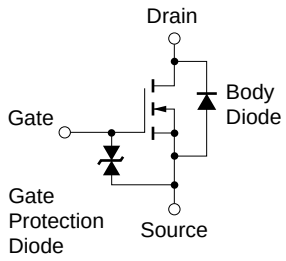
PACKAGE DRAWING (Unit : mm)

Power TSSOP8



Caution The terminal assignment is different from that of the NEC standard Power TSSOP8 package.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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